15-5 AN EXAMPLE OF AN IC OPERATIONAL AMPLIFIER

An integrated OP AMP usually consists of a cascade of four stages. As indicated in Fig. 15-10, the first stage is a DIFF AMP with a double-ended output, the second stage is a DIFF AMP with a single-ended output, the third stage is an emitter follower, and the last stage is a dc level translator and output driver.

In this section we examine in some detail an example[6] of an integrated operational amplifier, such as the Motorola MC1530 shown in Fig. 15-11. This amplifier is constructed to utilize the advantages of monolithic integrated circuits. It offers low offset voltage and current, small size, increased reliability, and excellent temperature tracking.

The purpose of this section is to analyze and evaluate the performance of this OP AMP.

Input Resistance The first stage, A_{V1}, consists of $Q2$ and $Q3$, with $Q1$ used as a constant-current source to provide high common-mode rejection. The differential input resistance R_{id} to the total input signal V_i is $2h_{ie}$, provided $R_s = 0$ and $h_{oe}R_c \leq 0.1$. This statement follows from the fact that, since $Q1$ acts as a constant current I_O, the emitters of $Q2$ and $Q3$ are floating. Hence the resistance between the two inputs 1 and 2 is $h_{ie2} + h_{ie3} = 2h_{ie}$. If input 2 is grounded, then input 1 is loaded by $2h_{ie}$.

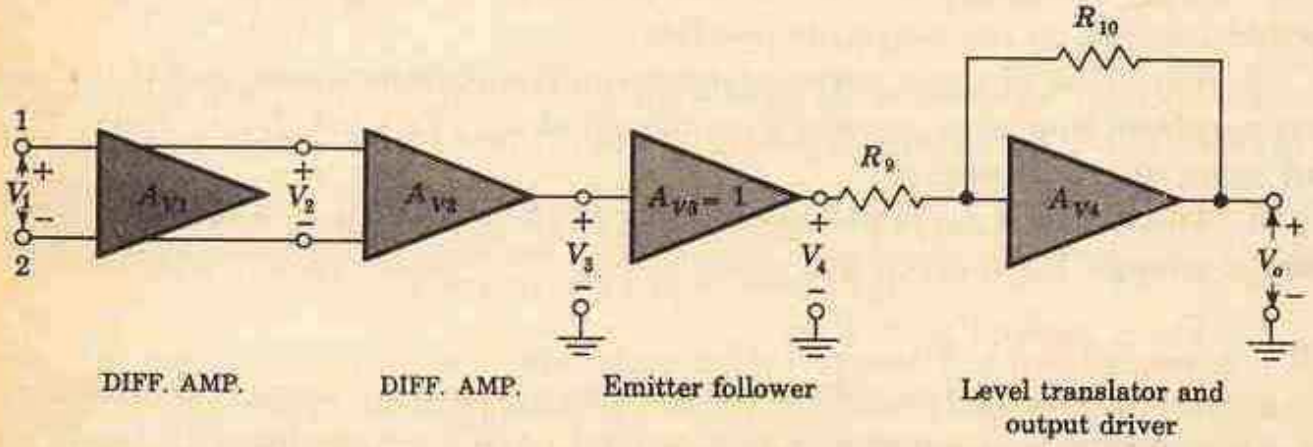

Fig. 15-10 The Motorola MC1530 as a four-stage cascaded amplifier.

If we neglect $r_{bb'}$ compared with $r_{b'e}$, then

$$h_{ie} \approx r_{b'e} = \frac{h_{fe}}{g_m} = \frac{h_{fe} V_T}{|I_C|} \tag{15-25}$$

where use is made of Eq. (11-11). We show further on in this section that $I_{C2} = I_{C3} = I_{C4} = I_{C5} \approx 0.5$ mA. Since $h_{fe} = 100$ for $Q2$ and $Q3$, the differential input resistance is

$$R_{id} = 2h_{ie} = \frac{2 \times 100 \times 26}{0.5} \Omega = 10.4 \text{ K}$$

If this resistance is too small for the applied signal source, it can be increased by modifying the input circuit. For example, some IC OP AMPS have a Darlington pair (Sec. 8-16) in place of $Q2$ and another in place of $Q3$. Another modification[7] is to add a matched discrete FET differential stage at the input, or preferably to fabricate an FET differential pair on the same chip with the rest of the OP AMP. Widlar[1] has designed OP AMPS (National Semiconductor Corp. LM108, for example) using supergain transistors (Sec. 7-6) in the input stage (current gains of 5,000 can be obtained at 1-μA collector current). For this transistor we find from Eq. (15-25)

$$h_{ie} = \frac{5{,}000 \times 26 \times 10^{-3}}{10^{-6}} \Omega = 130 \text{ M}$$

which is very high indeed for a bipolar transistor.

The differential input resistance of the second stage, consisting of the differential pair $Q4$ and $Q5$, is $2h_{ie}$. However, since double-ended signals are applied to $Q4$ and $Q5$, then the resistance looking into each base is half this value, or h_{ie}. This result follows from the equivalent circuit of Fig. 15-7*b*, which indicates that the emitter is effectively at ground potential. Since it is known that h_{fe} for transistor $Q4$ or $Q5$ is also 100, then $h_{ie} = 10.4/2 = 5.2$ K. This resistance is effectively connected from each collector of $Q2$ and $Q3$ to ground. Hence the equivalent collector-circuit load is

$$R_{L2} = R_{L3} = 7.75 \| 5.20 = 3.12 \text{ K}$$

Open-loop Voltage Gain The differential gain $A_d = A_{V1}$ is given by Eq. (15-14) multiplied by 2 (because the collector-to-collector output is twice the collector-to-ground output). Since $R_s = 0$, $h_{fe} = 100$, and

$$h_{ie} = 10.4/2 = 5.2 \text{ K}$$

for the first stage,

$$A_{V1} = \frac{V_2}{V_1} = \frac{h_{fe} R_{L2}}{h_{ie}} = \frac{100 \times 3.12}{5.20} = 60.0$$

For the second stage, $h_{fe} = 100$, $h_{ie} = 5.2$ K, and the load is $R_7 = 3$ K if we neglect the loading on $Q5$ of the emitter follower $Q6$ (whose input imped-

ance is high compared with 3 K). Since the second stage has a single-ended output, the differential gain is

$$A_{V2} = \frac{V_3}{V_2} = -\frac{1}{2}\frac{h_{fe}R_7}{h_{ie}} = -\frac{100 \times 3}{2 \times 5.2} = -28.9$$

For the emitter follower, $A_{V3} \approx 1$. The output stage uses voltage-shunt feedback because of R_9 and R_{10}. From Eq. (15-1)

$$A_{V4} \approx -\frac{R_{10}}{R_9} = -\frac{30}{6} = -5$$

Hence the overall OP AMP differential voltage gain is

$$A_V = (60.0)(-28.9)(-5) = +8{,}670$$

Note that node 1 is the noninverting input terminal.

DC Analysis It is necessary to know the dc currents and voltages of the circuit to obtain the open-loop gain and the differential input resistance and to understand the operation of the level-translator output stage.

Let us start with the current source $Q1$: We assume that all base currents can be neglected and all diode forward voltages and base-to-emitter voltages are 0.7 V. The dc voltage V_{BN1} of the base of $Q1$ with respect to ground N is (from Fig. 5-11)

$$V_{BN1} = \frac{[-V_{EE} + 2(0.7)]R_5}{R_4 + R_5} = \frac{(-6 + 1.4)(3.2)}{1.5 + 3.2} = -3.14 \text{ V}$$

and

$$I_O \approx I_1 = \frac{V_{EE} + (V_{BN1} - 0.7)}{R_1} = \frac{6 - 3.84}{2.2} = 0.99 \text{ mA}$$

If it is assumed that the integrated transistors $Q2$ and $Q3$ are identical, one-half of I_1 will flow through each:

$$I_{C2} = I_{C3} = 0.495 \text{ mA}$$

The dc voltage of the base of $Q4$ or $Q5$ with respect to ground is

$$V_{BN4} = V_{BN5} = V_{CC} - I_{C3}R_3 = 6 - 0.495 \times 7.75 \approx 2.18 \text{ V}$$

The dc voltage at the common emitter of $Q4$ and $Q5$ is

$$V_{EN4} = V_{BN4} - V_{BE4} = 2.18 - 0.7 = 1.48 \text{ V}$$

and the current in R_6 is

$$I_6 = \frac{V_{EN4}}{R_6} = \frac{1.48}{1.5} = 0.986 \text{ mA}$$

Since $I_6 = I_{C4} + I_{C5} = 2I_{C5}$, then $I_{C5} = 0.493$ and the base voltage of $Q6$, which equals the collector voltage V_3 of $Q5$, is

$$V_3 = V_{BN6} = V_{CN5} = V_{CC} - I_{C5}R_7 = 6 - (0.493)(3) = 4.52 \text{ V}$$

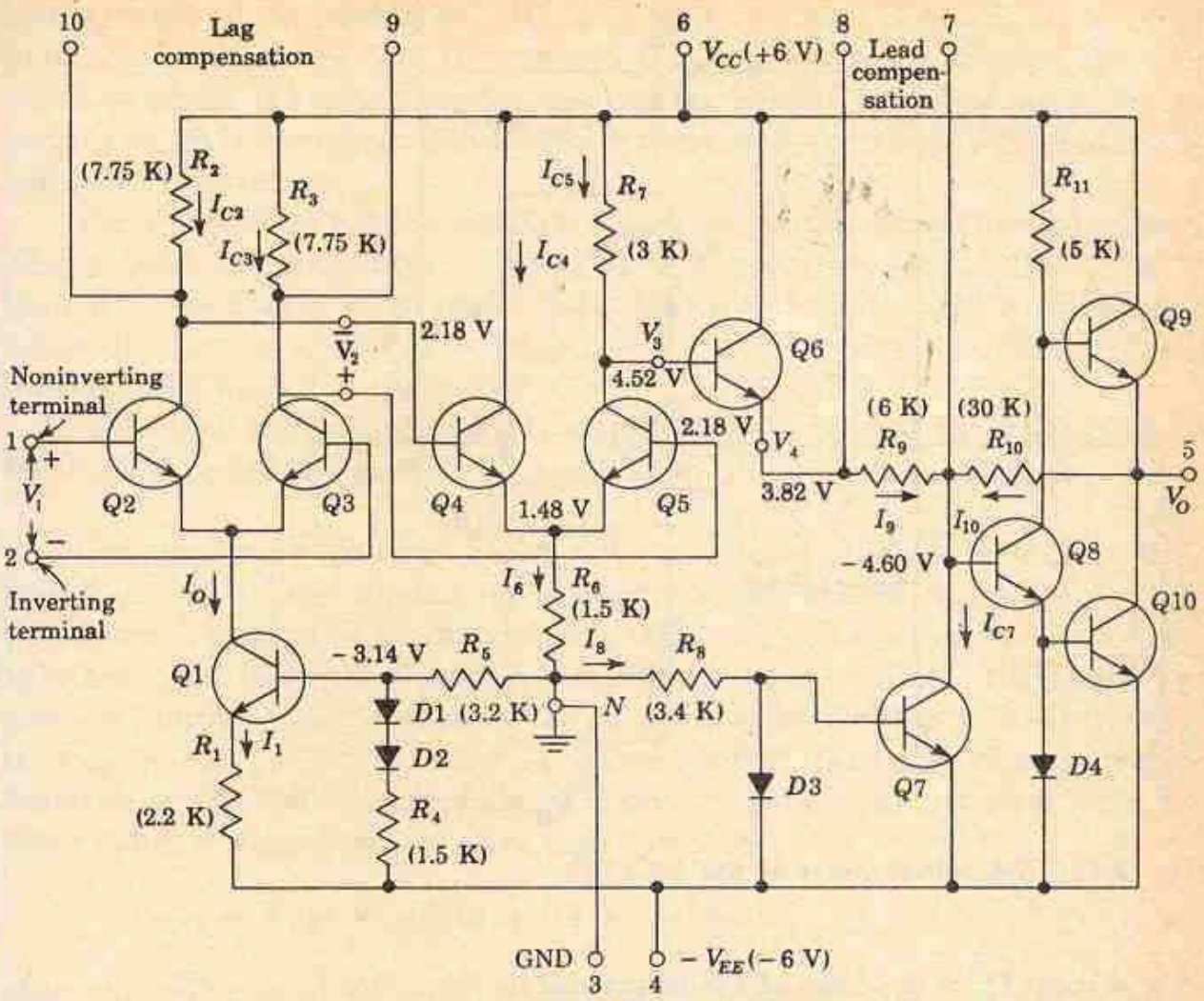

Fig. 15-11 The Motorola MC1530 operational amplifier. In the analysis all base currents are neglected.

The output V_4 of the emitter follower is

$$V_4 = V_{EN6} = V_{BN6} - V_{BE6} = 4.52 - 0.7 = 3.82 \text{ V}$$

The Output Stage The last stage provides level translation and a symmetrical output swing (at low impedance) with respect to ground. When the differential input voltage V_i is zero, the output V_o should be zero. Of course, due to mismatch of V_{BE} and h_{FE}, there will be some nonzero output voltage, which we consider in Sec. 15-7.

The voltage $V_{EN6} = 3.82$ V must be reduced to zero at the amplifier output while dc coupling is maintained. We shall now demonstrate that this level translation can be accomplished with the circuit parameter values in Fig. 15-11. Note that $Q7$ is biased by $D3$ in the manner explained in Sec. 9-7. Hence, following our discussion in Sec. 9-7 with respect to Fig. 9-11*a*, we find

$$I_{C7} \approx I_8 = \frac{V_{EE} - V_{D3}}{R_8} = \frac{6.0 - 0.7}{3.4} = 1.56 \text{ mA}$$

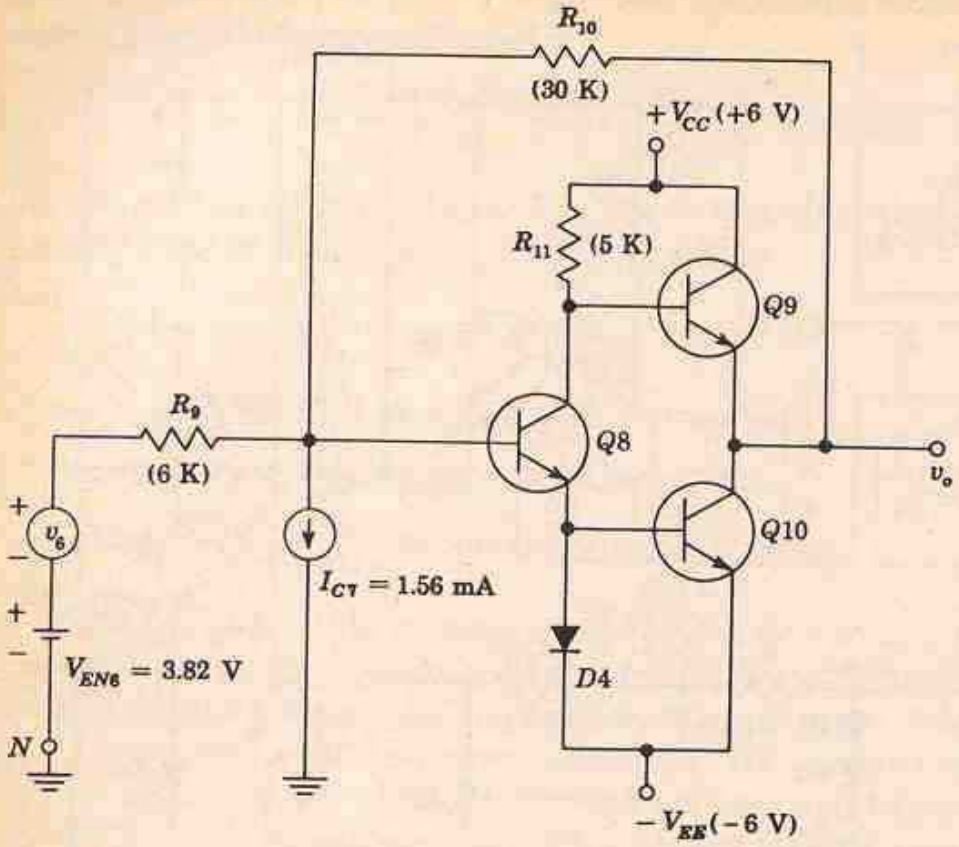

Fig. 15-12 The output stage of the MC1530.

The voltage from the base of $Q8$ to ground is

$$V_{BN8} = V_{BE8} + V_{D4} - V_{EE} = 0.7 + 0.7 - 6 = -4.60 \text{ V}$$

The currents in R_9 and R_{10} are

$$I_9 = \frac{V_{EN6} - V_{BN8}}{R_9} = \frac{3.82 + 4.60}{6} = 1.40 \text{ mA}$$

$$I_{10} = I_{C7} - I_9 = 1.56 - 1.40 = 0.16 \text{ mA}$$

Finally, the dc output voltage is

$$V_O = V_{BN8} + I_{10}R_{10} = -4.60 + (0.16)(30) = 0.20 \text{ V}$$

This calculated value for V_O is not to be taken too seriously, because we obtained I_{10} as the difference between two almost equal numbers. Such a subtraction can result in a large error in the small difference. Note that if I_{10} were 0.153 (instead of 0.16), then $V_O = 0$ (instead of 0.2 V). Also, I_{10} is greatly affected by small changes in the circuit parameter values. Hence a balancing technique (Sec. 15-6) is used to ensure that $V_O = 0$ for $V_i = 0$.

To consider the output stage under conditions of an applied excitation, refer to Fig. 15-12, where v_6 represents the signal voltage at the emitter of $Q6$, V_{EN6} is the dc voltage at this emitter, and I_{C7} is the constant current supplied by $Q7$. The signal v_6 is amplified by $Q8$ and is transmitted to the *totem-pole*

arrangement of $Q9$ and $Q10$. If v_6 is positive, then the current in $Q9$ is decreased and that in $Q10$ is increased, and current is taken from the load which is across the output and v_o decreases. Similarly, if v_6 is negative, the current in $Q9$ is increased, that in $Q10$ is decreased, current is delivered to the load, and v_o increases.

For a very large positive v_6, $Q9$ is cut off and $Q10$ is driven into saturation. Under these circumstances $v_o = -V_{BE} + V_{CE10,sat} = -6 + 0.2 = -5.8$ V. Similarly, for a very large negative v_6, $Q10$ is cut off and $Q9$ is driven into saturation, so that $v_o = V_{CC} - V_{CE9,sat} = 6 - 0.2 = +5.8$ V. The maximum peak-to-peak output swing is 11.6 V.

Note that the output stage is stabilized by means of the voltage-shunt feedback supplied by resistors R_9 and R_{10}.

Common-mode Voltage Swing We are going to show now that V_{BN1} and V_{CN2} set a limit on the input *common-mode voltage swing* V_{iCM}. This parameter is defined as the maximum peak input voltage that can be applied to either input terminal without causing abnormal operation or damage. The positive limit of V_{iCM} depends on the collector voltage of the input stage; that is, $V_{CN2} = V_{BN4} \approx 2.2$ V. If V_{iCM} exceeds 2.2 V, then the collector-to-base junction of $Q2$ will become forward biased and $Q2$ may saturate. On the other hand, if V_{iCM} becomes more negative than

$$V_{BN1} + V_{BE2} = -3.14 + 0.7 = -2.44 \text{ V}$$

then the collector of $Q1$ will become forward biased, and this will result in abnormal operation. Therefore, when the power supplies are ± 6 V, the common-mode voltage swing for this amplifier should not exceed ± 2 V maximum.