15-2 THE DIFFERENTIAL AMPLIFIER

The function of a differential amplifier[4] (abbreviated DIFF AMP) is, in general, to amplify the difference between two signals. The need for DIFF AMPS arises in many physical measurements where response from dc to many megahertz is required. It is also the basic stage of an integrated operational amplifier with differential input.

Figure 15-5 represents a linear active device with two input signals v_1, v_2 and one output signal v_o, each measured with respect to ground. In an ideal DIFF AMP the output signal v_o should be given by

$$v_o = A_d(v_1 - v_2) \tag{15-5}$$

where A_d is the gain of the differential amplifier. Thus it is seen that any signal which is common to both inputs will have no effect on the output voltage. However, a practical DIFF AMP cannot be described by Eq. (15-5), because, in general, the output depends not only upon the *difference signal* v_d of the two signals, but also upon the average level, called the *common-mode signal* v_c, where

$$v_d \equiv v_1 - v_2 \qquad \text{and} \qquad v_c \equiv \tfrac{1}{2}(v_1 + v_2) \tag{15-6}$$

For example, if one signal is $+50\ \mu V$ and the second is $-50\ \mu V$, the output will not be exactly the same as if $v_1 = 1{,}050\ \mu V$ and $v_2 = 950\ \mu V$, even though the difference $v_d = 100\ \mu V$ is the same in the two cases.

The Common-mode Rejection Ratio The foregoing statements are now clarified, and a figure of merit for a difference amplifier is introduced. The output of Fig. 15-5 can be expressed as a linear combination of the two input voltages

$$v_o = A_1 v_1 + A_2 v_2 \tag{15-7}$$

where $A_1(A_2)$ is the voltage amplification from input 1(2) to the output under the condition that input 2(1) is grounded. From Eqs. (15-6)

$$v_1 = v_c + \tfrac{1}{2}v_d \qquad \text{and} \qquad v_2 = v_c - \tfrac{1}{2}v_d \tag{15-8}$$

If these equations are substituted in Eq. (15-7), we obtain

$$v_o = A_d v_d + A_c v_c \tag{15-9}$$

where

$$A_d \equiv \tfrac{1}{2}(A_1 - A_2) \qquad \text{and} \qquad A_c \equiv A_1 + A_2 \tag{15-10}$$

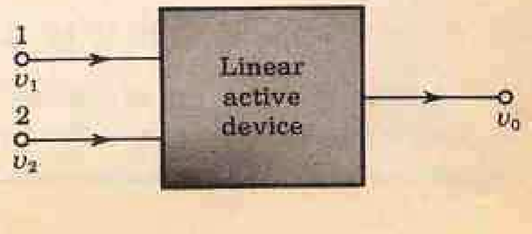

Fig. 15-5 The output is a linear function of v_1 and v_2 for an ideal differential amplifier; $v_o = A_d(v_1 - v_2)$.

The voltage gain for the difference signal is A_d, and that for the common-mode signal is A_c. We can measure A_d directly by setting $v_1 = -v_2 = 0.5$ V, so that $v_d = 1$ V and $v_c = 0$. Under these conditions the measured output voltage v_o gives the gain A_d for the difference signal [Eq. (15-9)]. Similarly, if we set $v_1 = v_2 = 1$ V, then $v_d = 0$, $v_c = 1$ V, and $v_o = A_c$. The output voltage now is a direct measurement of the common-mode gain A_c.

Clearly, we should like to have A_d large, whereas ideally, A_c should equal zero. A quantity called the *common-mode rejection ratio*, which serves as a figure of merit for a DIFF AMP, is defined by

$$\text{CMRR} \equiv \rho \equiv \left| \frac{A_d}{A_c} \right| \tag{15-11}$$

From Eqs. (15-9) and (15-11) we obtain an expression for the output in the following form:

$$v_o = A_d v_d \left(1 + \frac{1}{\rho} \frac{v_c}{v_d} \right) \tag{15-12}$$

From this equation we see that the amplifier should be designed so that ρ is large compared with the ratio of the common-mode signal to the difference signal. For example, if $\rho = 1{,}000$, $v_c = 1$ mV, and $v_d = 1\ \mu$V, the second term in Eq. (15-12) is equal to the first term. Hence, for an amplifier with a common-mode rejection ratio of 1,000, a 1-μV difference of potential between the two inputs gives the same output as a 1-mV signal applied with the same polarity to both inputs.

EXAMPLE (*a*) Consider the situation referred to above, where the first set of signals is $v_1 = +50\ \mu$V and $v_2 = -50\ \mu$V and the second set is $v_1 = 1{,}050\ \mu$V and $v_2 = 950\ \mu$V. If the common-mode rejection ratio is 100, calculate the percentage difference in output voltage obtained for the two sets of input signals. (*b*) Repeat part *a* if $\rho = 10{,}000$.

Solution *a*. In the first case, $v_d = 100\ \mu$V and $v_c = 0$, so that, from Eq. (15-12), $v_o = 100A_d \quad \mu$V.

In the second case, $v_d = 100\ \mu$V, the same value as in part *a*, but now $v_c = \frac{1}{2}(1{,}050 + 950) = 1{,}000\ \mu$V, so that, from Eq. (15-12),

$$v_o = 100A_d\left(1 + \frac{10}{\rho}\right) = 100A_d\left(1 + \frac{10}{100}\right) \quad \mu\text{V}$$

These two measurements differ by 10 percent.

b. For $\rho = 10{,}000$, the second set of signals results in an output

$$v_o = 100A_d(1 + 10 \times 10^{-4}) \quad \mu\text{V}$$

whereas the first set of signals gives an output $v_o = 100A_d \quad \mu$V. Hence the two measurements now differ by only 0.1 percent.

15-3 THE EMITTER–COUPLED DIFFERENTIAL AMPLIFIER

The circuit of Fig. 15-6 is an excellent DIFF AMP if the emitter resistance R_e is large. This statement can be justified as follows: If $V_{s1} = V_{s2} = V_s$, then from Eqs. (15-6) and (15-9) we have $V_d = V_{s1} - V_{s2} = 0$ and $V_o = A_c V_s$. However, if $R_e = \infty$, then, because of the symmetry of Fig. 15-6, we obtain $I_{e1} = I_{e2} = 0$. Since $I_{b2} \ll I_{c2}$, then $I_{c2} \approx I_{e2}$, and it follows that $V_o = 0$. Hence the common-mode gain A_c becomes zero, and the common-mode rejection ratio is infinite for $R_e = \infty$ and a symmetrical circuit.

We now analyze the emitter-coupled circuit for a finite value of R_e. A_c can be evaluated by setting $V_{s1} = V_{s2} = V_s$ and making use of the symmetry of Fig. 15-6. This circuit can be bisected as in Fig. 15-7*a*. An analysis of this circuit (Prob. 15-10), using Eqs. (8-67) to (8-69) and neglecting the term in h_{re} in Eq. (8-68), yields

$$A_c = \frac{V_o}{V_s} = \frac{(2h_{oe}R_e - h_{fe})R_c}{2R_e(1 + h_{fe}) + (R_s + h_{ie})(2h_{oe}R_e + 1)} \tag{15-13}$$

provided that $h_{oe}R_c \ll 1$. Similarly, the difference mode gain A_d can be obtained by setting $V_{s1} = -V_{s2} = V_s/2$. From the symmetry of Fig. 15-6. we see that, if $V_{s1} = -V_{s2}$, then the emitter of each transistor is grounded for small-signal operation. Under these conditions the circuit of Fig. 15-7*b* can be used to obtain A_d. Hence

$$A_d = \frac{V_o}{V_s} = \frac{1}{2}\frac{h_{fe}R_c}{R_s + h_{ie}} \tag{15-14}$$

provided $h_{oe}R_c \ll 1$. The common-mode rejection ratio can now be obtained using Eqs. (15-11), (15-13), and (15-14).

From Eq. (15-13) it is seen that the common-mode rejection ratio increases with R_e, as predicted above. There are, however, practical limitations on the magnitude of R_e because of the quiescent dc voltage drop across it; the emitter

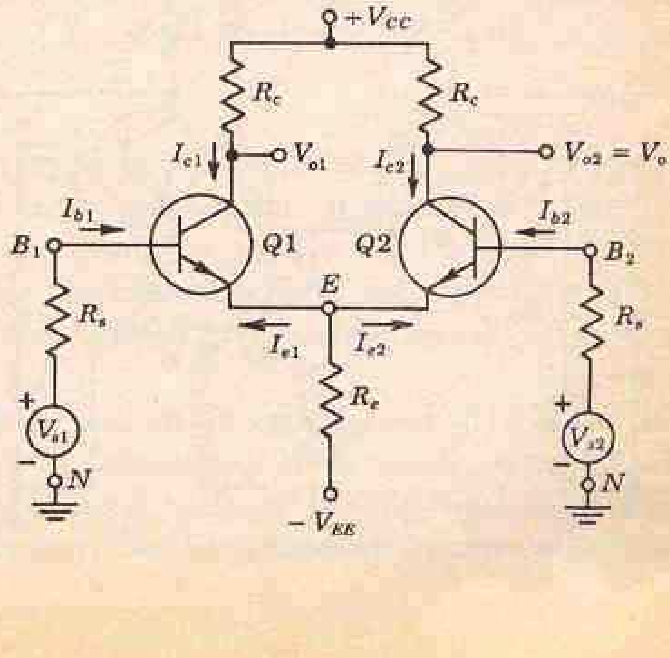

Fig. 15-6 Symmetrical emitter-coupled difference amplifier.

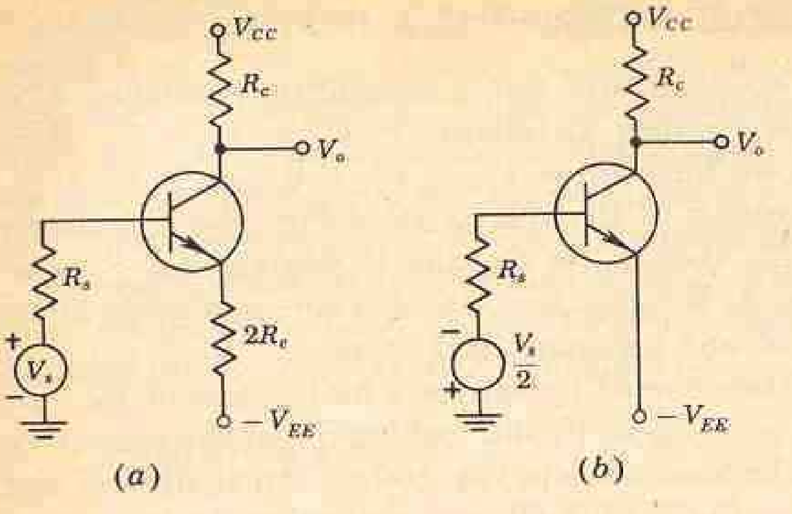

Fig. 15-7 Equivalent circuit for a symmetrical differential amplifier used to determine (a) the common-mode gain A_c and (b) the difference gain A_d.

supply V_{EE} must become larger as R_e is increased, in order to maintain the quiescent current at its proper value. If the operating currents of the transistors are allowed to decrease, this will lead to higher h_{ie} values and lower values of h_{fe}. Both of these effects will tend to decrease the common-mode rejection ratio.

Differential Amplifier Supplied with a Constant Current Frequently, in practice, R_e is replaced by a transistor circuit, as in Fig. 15-8, in which R_1, R_2, and R_3 can be adjusted to give the same quiescent conditions for $Q1$ and $Q2$ as the original circuit of Fig. 15-6. This modified circuit of Fig. 15-8 presents a very high effective emitter resistance R_e for the two transistors $Q1$ and $Q2$. Since R_e is also the effective resistance looking into the collector of transistor $Q3$, it is given by Eq. (8-70). In Sec. 8-15 it is verified that R_e is hundreds of kilohms even if R_3 is as small as 1 K.

We now verify that transistor $Q3$ acts as an approximately constant cur-

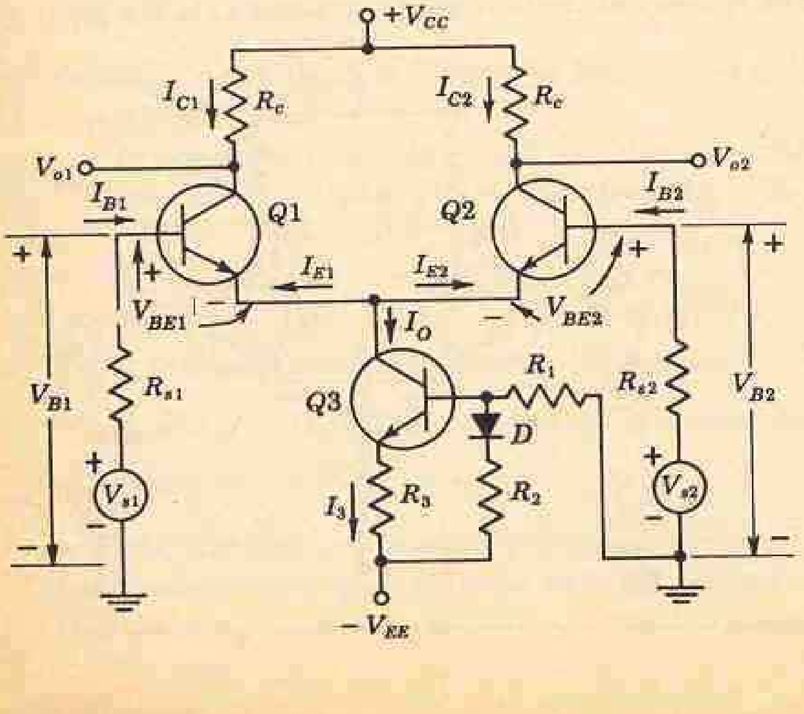

Fig. 15-8 Differential amplifier with constant-current stage in the emitter circuit. Nominally, $R_{s1} = R_{s2}$.

rent source, subject to the condition that the base current of $Q3$ is negligible. Applying KVL to the base circuit of $Q3$, we have

$$I_3R_3 + V_{BE3} = V_D + (V_{EE} - V_D)\frac{R_2}{R_1 + R_2} \tag{15-15}$$

where V_D is the diode voltage. Hence

$$I_O \approx I_3 = \frac{1}{R_3}\left(\frac{V_{EE}R_2}{R_1 + R_2} + \frac{V_DR_1}{R_1 + R_2} - V_{BE3}\right) \tag{15-16}$$

If the circuit parameters are chosen so that

$$\frac{V_DR_1}{R_1 + R_2} = V_{BE3} \tag{15-17}$$

then

$$I_O = \frac{V_{EE}R_2}{R_3(R_1 + R_2)} \tag{15-18}$$

Since this current is independent of the signal voltages V_{s1} and V_{s2}, then $Q3$ acts to supply the DIFF AMP consisting of $Q1$ and $Q2$ with the constant current I_O.

The above result for I_O has been rendered independent of temperature because of the added diode D. Without D the current would vary with temperature because V_{BE3} decreases approximately 2.5 mV/°C (Sec. 5-8). The diode has this same temperature dependence, and hence the two variations cancel each other and I_O does not vary appreciably with temperature. Since the cutin voltage V_D of a diode has approximately the same value as the base-to-emitter voltage V_{BE3} of a transistor, then Eq. (15-17) cannot be satisfied with a single diode. Hence two diodes in series are used for V_D (Fig. 15-11).

Consider that $Q1$ and $Q2$ are identical and that $Q3$ is a true constant-current source. Under these circumstances we can demonstrate that the common-mode gain is zero. Assume that $V_{s1} = V_{s2} = V_s$, so that from the symmetry of the circuit, the collector current I_{c1} (the increase over the quiescent value for $V_s = 0$) in $Q1$ equals the current I_{c2} in $Q2$. However, since the total current increase $I_{c1} + I_{c2} = 0$ if I_O = constant, then $I_{c1} = I_{c2} = 0$ and $A_c = V_{o2}/V_s = -I_{c2}R_c/V_s = 0$.

Practical Considerations[4] In some applications the choice of V_{s1} and V_{s2} as the input voltages is not realistic because the resistances R_{s1} and R_{s2} represent the output impedances of the voltage generators V_{s1} and V_{s2}. In such a case we use as input voltages the base-to-ground voltages V_{b1} and V_{b2} of $Q1$ and $Q2$, respectively. For the analysis of nonsymmetrical differential circuits the reader is referred to Ref. 4.

The differential amplifier is often used in dc applications. It is difficult to design dc amplifiers using transistors because of drift due to variations of h_{FE}, V_{BE}, and I_{CBO} with temperature. A shift in any of these quantities changes the output voltage and cannot be distinguished from a change in input-signal voltage. Using the techniques of integrated circuits (Chap. 7), it is possible to construct a DIFF AMP with $Q1$ and $Q2$ having almost identical characteristics. Under these conditions any parameter changes due to temperature will cancel and the output will not vary.

Differential amplifiers may be cascaded to obtain larger amplifications for the difference signal. Outputs V_{o1} and V_{o2} are taken from each collector (Fig. 15-8) and are coupled directly to the two bases, respectively, of the next stage (Fig. 15-11).

Finally, the differential amplifier may be used as an emitter-coupled phase inverter. For this application the signal is applied to one base, whereas the second base is not excited (but is, of course, properly biased). The output voltages taken from the collectors are equal in magnitude and 180° out of phase.

15-4 TRANSFER CHARACTERISTICS OF A DIFFERENTIAL AMPLIFIER

It is important to examine the transfer characteristic[5] (I_C versus $V_{B1} - V_{B2}$) of the DIFF AMP of Fig. 15-8 to understand its advantages and limitations. We first consider this circuit qualitatively. When V_{B1} is below the cutoff point of $Q1$, all the current I_O flows through $Q2$ (assume for this discussion that V_{B2} is constant). As V_{B1} carries $Q1$ above cutoff, the current in $Q1$ increases, while the current in $Q2$ decreases, and the sum of the currents in the two transistors remain constant and equal to I_O. The total range ΔV_O over which the output can follow the input is $R_C I_O$ and is therefore adjustable through an adjustment of I_O.

From Fig. 15-8 we have

$$I_{E1} + I_{E2} = -I_O \tag{15-19}$$

$$V_{B1} - V_{B2} = V_{BE1} - V_{BE2} \tag{15-20}$$

The emitter current I_E of each transistor is related to the voltage V_{BE} by the diode volt-ampere characteristic

$$I_E = I_S \epsilon^{V_{BE}/V_T} \tag{15-21}$$

where I_S is defined in terms of the Ebers-Moll parameters in Prob. 15-12.

If we assume that $Q1$ and $Q2$ are matched, it follows from Eqs. (15-19) to (15-21) that

$$I_{C1} \approx -I_{E1} = \frac{I_O}{1 + \exp\left[-(V_{B1} - V_{B2})/V_T\right]} \tag{15-22}$$

and I_{C2} is given by the same expression with V_{B1} and V_{B2} interchanged. The transfer characteristics described by Eq. (15-22) for the normalized collector currents I_{C1}/I_O (and I_{C2}/I_O) are shown in Fig. 15-9, where the abscissa is the normalized differential input $(V_{B1} - V_{B2})/V_T$.

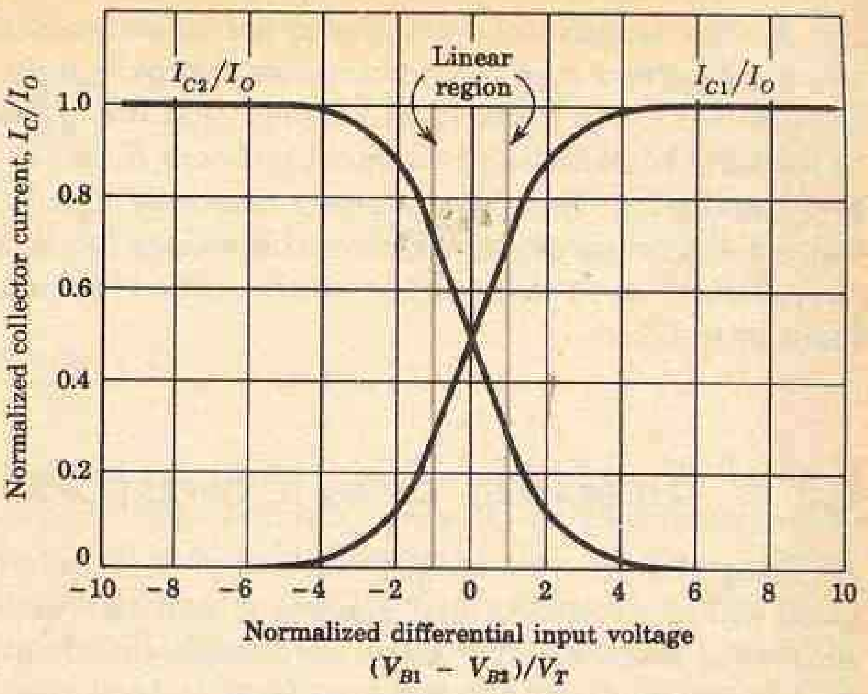

Fig. 15-9 Transfer characteristics of the basic differential-amplifier circuit.

If Eq. (15-22) is differentiated with respect to $V_{B1} - V_{B2}$, we have the transconductance g_{md} of the DIFF AMP with respect to the differential input voltage, or

$$\frac{dI_{C1}}{d(V_{B1} - V_{B2})} = g_{md} = \frac{I_O}{4V_T} \tag{15-23}$$

where g_{md} is evaluated at $V_{B1} = V_{B2}$. This equation indicates that, for the same value of I_O, the effective transconductance of the differential amplifier is one-fourth that of a single transistor [Eq. (11-4)]. An alternative proof of Eq. (15-23) is given in Prob. 15-11.

The following conclusions can be drawn from the transfer curves of Fig. 15-9:

1. The differential amplifier is a very good limiter, since when the input $(V_{B1} - V_{B2})$ exceeds $\pm 4V_T$ ($\approx \pm 100$ mV at room temperature), very little further increase in the output is possible.

2. The slope of these curves defines the transconductance, and it is clear that g_{md} starts from zero, reaches a maximum of $I_O/4V_T$ when $I_{C1} = I_{C2} = \frac{1}{2}I_O$, and again approaches zero.

3. The value of g_{md} is proportional to I_O [Eq. (15-23)]. Since the output voltage change V_{o2} is given by

$$V_{o2} = g_{md}R_c(V_{B1} - V_{B2}) \tag{15-24}$$

it is possible to change the differential gain by varying the value of the current I_O. This means that automatic gain control (AGC) is possible with the DIFF AMP.

4. The transfer characteristics are linear in a small region around the operating point where the input varies approximately $\pm V_T$ (± 26 mV at room temperature). In Prob. 15-14 we show that it is possible to increase the region of linearity by inserting two equal resistors R_e in series with the emitter leads of $Q1$ and $Q2$. This current-series feedback added to each transistor results in a smaller value of g_{md}. Reasonable values for R_e are $50 - 100\ \Omega$, since for large values, A_d is reduced too much. The insertion of R_e also increases the input impedance.